REPLACEMENT CLAIMS

Please cancel claims 1-13.

Please add the following claims 14-22.

A2

14. (New Claim) A semiconductor package array comprising:
an interconnect substrate having a plurality of substantially identical package sites arranged in an array, the plurality of sites being separated by a singulation space;
a semiconductor device mounted within each site and interconnected thereto; and
a single and continuous overmolded encapsulant material which encapsulates each semiconductor device, the plurality of sites, and the singulation space.

15. (New Claim) The semiconductor package array of claim 14 wherein a top surface of the overmolded encapsulant material has a surface deviation of less than 0.13 millimeters across a length of the encapsulant material.

16. (New Claim) The semiconductor package array of claim 14 wherein the plurality of package sites are arranged in an array of at least four by four package sites.

17. (New Claim) A method for making a packaged semiconductor device comprising:
providing an interconnect substrate having a plurality of substantially identical package sites arranged in an array, the plurality of sites being separated by a singulation space;
mounting and interconnecting a semiconductor device within each site; and
overmolding a single and continuous encapsulant over each semiconductor device, the plurality of sites, and the singulation space.

18. (New Claim) The method of claim 17 wherein overmolding produces a top surface of the encapsulant which has a surface deviation of less than 0.13 millimeters across a length of the encapsulant.

19. (New Claim) The method of claim 17 wherein providing an interconnect substrate comprises providing an interconnect substrate wherein the plurality of package sites are arranged in an array of at least four by four package sites.

20. (New Claim) The method of claim 17 further comprising the step of singulating the plurality of package sites after overmolding.